AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) Apparatus for managing flow of information among plural processors of a processing array, comprising:

a plurality of processors, each processor being in communication with a respective local processor bus;

a system bus for interconnecting at least two processors and providing a path for packets of data and control information, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus; and

means for arbitrating access to at least a first portion of the system bus among said at least two processors to transfer said packets of data and control information over said first portion, said means for arbitrating establishing a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy, and said packets being transferred using a protocol by which the system bus performs control actions for system bus access independently of said at least two processors.

2. (Original) The apparatus of claim 1, comprising:

at least one module connected by said system bus to said means for arbitrating.

3. (Original) The apparatus of claim 2, wherein said at least one module comprises a gateway device for communicating via said system bus to said means for arbitration.

4. (Original) The apparatus of claim 3, wherein said at least one module comprises a module bus for administering to at least one module node within said at least one module.

5. (Original) The apparatus of claim 4, wherein said at least one module node comprises a processing device.

6. (Original) The apparatus of claim 5, wherein said at least one module node comprises a bus interface device for achieving data communication between said processing device and said module bus.

7. (Original) The apparatus of claim 6, wherein said at least one module comprises a local processor bus for communicating data between said processing device and said bus interface device.

8. (Original) The apparatus of claim 1, comprising:

a sensor interface connected to said system bus.

9. (Original) The apparatus of claim 8, wherein said sensor interface comprises a processor for processing sensor data.

10. (Original) The apparatus of claim 9, wherein said sensor interface comprises a bus interface device for communicating data between said processor and said system bus.

11. (Original) The apparatus of claim 10, wherein said sensor interface comprises a local processor bus for communicating data between said processor and said bus interface device.

12. (Original) The apparatus of claim 8, wherein said sensor interface comprises a video sensor interface.

13. (Original) The apparatus of claim 8, wherein said sensor interface comprises a forward looking infrared (FLIR) sensor interface.

14. (Original) The apparatus of claim 1, comprising a system controller for controlling access to the system bus.

15. (Original) The apparatus of claim 14, wherein said system controller comprises a system bus arbitration unit for controlling access to the system bus.

16. (Original) The apparatus of claim 14, wherein said system controller comprises a processor connected to a bus interface device, which is connected to the system bus.

17. (Currently Amended) A method for managing flow of information among plural processors of a processing array, comprising the steps of:

providing a local connection by a local processor bus for each of a plurality of processors;

interconnecting at least two processors for providing a path for packets of data and control information by a system bus, control information packets being separately buffered from other packets in a buffer separately connected between the respective local processor bus and the system bus; and

arbitrating access to at least a first portion of a system bus among said at least two processors to transfer said packets of data and control information over said first portion, said packets being transferred using a protocol by which a system bus performs control actions for system bus access independently of said at least two processors, wherein arbitrating access comprises establishing a clear path to a destination device by checking device busy signals to ensure that the destination device is not busy.

18. (Original) The method of claim 17, comprising the step of:

interconnecting at least one module with said system bus by way of a bus gateway device, said at least one module comprising said bus gateway device, a

module bus, at least one processor, and at least one bus interface device for connecting said at least one processor to said module bus.

19. (Previously Presented) The method of claim 18, wherein said step of arbitrating comprises the steps of:

requesting a bus grant to transmit data packets to said device;

receiving a bus grant signal in response to said step of requesting, indicating that data may be transmitted over the system bus; and

transmitting data packets in response to said step of receiving.

20. (Currently Amended) The method of ~~step~~ claim 19, wherein said steps of requesting and receiving are accomplished by a device connected to the system bus.

21. (Currently Amended) The method of ~~step~~ claim 20, wherein said bus grant signal is issued by a system bus arbitration unit.

22. (Currently Amended) The method of ~~step~~ claim 17, wherein said step of arbitrating comprises the steps of:

inquiring if the system bus is in use;

verifying that a destination device is not busy once the system bus is not in use;

requesting access to the system bus to a system bus arbitration unit;

gaining access to the system bus from said system bus arbitration unit; and

transmitting data packets to said destination device.

23. (Currently Amended) The method of ~~step~~ claim 22, wherein the system bus arbitration unit allows continual access to the system bus if the destination device does not become busy, if the bus does not become busy, and if no other device requests access to the system bus.

24. (Currently Amended) The method of ~~step~~ claim 23, wherein the system bus arbitration unit grants access to a second device upon request during a transmission of a data packet by another device on the system bus.

25. (Original) The method of claim 24, wherein access to the system bus is granted to a second device by the system bus arbitration unit, which executes the steps of:

discontinuing bus grant access to any device currently transmitting data;

verifying that the system bus is not busy;

verifying that a destination device is not busy;

granting access to the system bus for the second device requesting access;

delaying any further transmission by said device whose access to the system bus was discontinued by said step of discontinuing until after at least one data packet has been transmitted by said second device.

26. (Original) The method of claim 25, wherein access to the system bus between multiple devices connected to the system bus is granted according to priority.

27. (Previously Presented) The method of claim 26, wherein access to the system bus between multiple devices connected to the system bus is granted in a rotating fashion based on said priority and for a maximum of time required to transfer one data packet.

28. (Original) The method of claim 17, wherein devices connected to the system bus contain local and module busses connected to the system bus by way of a gateway device, which arbitrates access to nodes connected to said module bus.

29. (Original) The method of claim 28, wherein said gateway device arbitrates access to the local and module busses according to priority.

30. (Original) The method of claim 29, wherein said gateway device arbitrates access to the local and module busses in a rotating fashion.

31. (Previously Presented) The method of claim 28, wherein arbitration of access to the module bus is accomplished by the following steps:

inquiring if the module bus is in use;

verifying that a destination processor is not busy once the module bus is not in use;

requesting access to the module bus to a bus gateway device;

gaining access to the module bus from said bus gateway device; and

transmitting data packets to said destination processor.